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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCESIn re Application of: Rajesh Khamankar, *et al.*

Serial No.: 10/702,234

Filed: November 6, 2003

Title: **RELIABLE HIGH VOLTAGE GATE DIELECTRIC
LAYERS USING A DUAL NITRIDATION PROCESS**

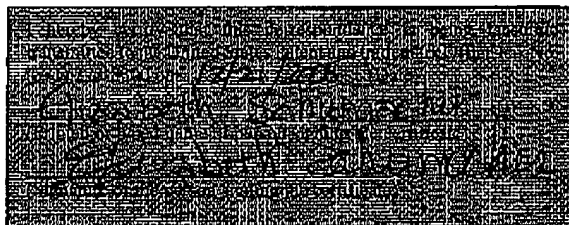
Grp./A.U.: 2814

Examiner: Nathan W. Ha

ATTENTION: Board of Patent Appeals and Interferences

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Sirs:

**APPEAL BRIEF UNDER 37 C.F.R. §41.37**

This is an appeal from a Final Rejection dated June 10, 2005, of Claims 1-8. The Appellants submit this Brief with the statutory fee of a large entity as set forth in 37 C.F.R. §41.20(b)(2), and hereby authorize the Commissioner to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 20-0668.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §41.37(c)(1):

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- I. REAL PARTY IN INTEREST
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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Texas Instruments, Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-8 are pending in this application and have been rejected under 35 U.S.C §§102, 103. Each of the pending claims is being appealed.

IV. STATUS OF THE AMENDMENTS

The present Application was filed on November 6, 2003. The Appellants filed a preliminary amendment on November 6, 2003. The Appellants then filed an Election on October 5, 2004, in response to an Examiner's Restriction Requirement mailed on September 9, 2004. The Appellants then filed a first Amendment on March 18, 2005, in response to a first Examiner's Action mailed on December 20, 2004. The Examiner entered the first Amendment and subsequently issued a Final Rejection on June 10, 2005. The Appellants then filed a second Amendment on September 2, 2005. The Examiner indicated that the second Amendment had been entered, but did not place the Application in condition for allowance. The Appellants then filed a Notice of Appeal on October 3, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed, in general, to a method for forming dual gate (or split gate) dielectrics for integrated circuit MOS transistors using a dual plasma nitridation process. (See page 1, lines 5-8).

Independent Claim 1 is directed to a method for forming MOS transistor gate dielectrics, including: (1) providing a semiconductor substrate, (2) forming a first dielectric layer on the semiconductor substrate, (3) performing a first plasma nitridation of the first dielectric layer, (4) removing the first dielectric from a region of the substrate, (5) forming a second dielectric layer on the semiconductor substrate in the region from which the first dielectric layer was removed, and (6) simultaneously performing a second plasma nitridation of the second dielectric layer and the first dielectric layer.

Independent Claim 6 is directed to a method for forming integrated circuit MOS transistors, including: (1) providing a semiconductor substrate, (2) forming a first silicon oxide layer, (3) performing a plasma nitridation process on said first silicon oxide layer forming a first plasma nitrided oxide layer, (4) removing said first plasma nitrided oxide layer from regions of said substrate, and (5) forming a second plasma nitrided oxide layer on said semiconductor substrate in said regions from which said first plasma nitrided oxide layer was removed.

In one embodiment, a first dielectric layer 30 is formed on a substrate 10. The first dielectric layer 30 may then be subjected to a first plasma nitridation process. (See paragraph [0010] of the published application). Following the formation of the first dielectric layer 30 and the subsequent first plasma nitridation treatment, a patterned photoresist layer 40 is formed over the first dielectric layer. (See paragraph [0011] of the published application). The portions of the first dielectric layer 30 not covered by the patterned photoresist layer 40 are then removed using standard techniques such as etching in 0.49% buffered hydrogen fluoride. (See paragraph [0011] of the published application). Following the removal of the exposed first dielectric layer, the patterned photoresist layer 40 is removed. (See paragraph [0011] of the published application).

Thereafter, a second dielectric layer 50 is formed on the surface of the substrate in those regions where the first dielectric layer was removed. (See paragraph [0012] of the published application). Following the formation of the silicon oxide layer a second plasma nitridation process is performed. (See paragraph [0012] of the published application). During the formation of the plasma nitrided dielectric layer 50, the dielectric layer 30 is exposed to all the processes. (See paragraph [0013] of the published application).

During the growth of the second dielectric layer 50, additional oxide growth will take place in the remaining region of the first dielectric layer 30. (See paragraph [0013] of the published application). In addition, the first dielectric layer will be exposed to the second plasma nitridation process of the second dielectric layer. (See paragraph [0013] of the published application). Therefore the first dielectric layer 30 undergoes dual nitridation treatments. (See paragraph [0013] of the published application).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The first issue presented for consideration in this appeal is whether Claims 1-3 and 6-7, as rejected by the Examiner, are anticipated in accordance with 35 U.S.C. §102(e) by U.S. Patent No. 6,716,685 to Lahaug ("Lahaug").

(B) The second issue presented for consideration in this appeal is whether Claims 4-5 and 8, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over Lahaug as applied to Claims 1-3 and 6-7 above, and further in view of U.S. Patent No. 6,087,236 to Chau, *et al.* ("Chau").

VII. APPELLANTS' ARGUMENT

The inventions set forth in independent Claims 1 and 6 and their respective dependent claims are neither anticipated by nor obvious over the references on which the Examiner relies.

Rejection under 35 U.S.C. 102(e) over Lahaug

B. Rejection of Claims 1-3 and 6-7.

The Examiner has rejected Claims 1-3 and 6-7 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,716,685 to Lahaug ("Lahaug"). The Appellants respectfully disagree since Lahaug fails to disclose the element of performing a second plasma nitridation process on the second oxide layer and the first plasma nitrided oxide layer, with respect to Claim 1, and forming a second plasma nitrided oxide layer on the semiconductor substrate in the regions from which the first plasma nitrided oxide layer was removed, with respect to Claim 6.

The Examiner argues that Lahaug teaches simultaneously performing a second plasma nitridation, "reoxidation", of the second dielectric layer and the first dielectric layer. In making this argument, the Examiner only points the Appellants to column 4, lines 5-14, of the Lahaug reference. However, the Lahaug reference, at the supplied column and line, makes no such teaching. Actually, the Lahaug reference fails to provide any teaching, at any column and line, of subjecting the second oxide layer to a plasma nitridation process (e.g., with respect to independent Claim 1), or forming a second plasma nitrided oxide layer (e.g., with respect to independent Claim 6). The Lahaug reference clearly only discloses subjecting the first gate oxide layer 18 to a first plasma nitridation process, thereby forming the oxynitride layer 20. As Lahaug's first plasma nitridation process is conducted before the formation of its second gate oxide layer 30, it cannot be performed on the second gate oxide layer 30, as claimed in independent Claim 1. Moreover, as the first plasma nitridation process is the only nitridation process disclosed in Lahaug, the second gate oxide layer 30 cannot be a second plasma nitrided oxide layer, as claimed in independent Claim 6. Accordingly, Lahaug fails to disclose these claimed elements.

The Examiner may be misinterpreting the term "reoxidation" used at column 4, lines 5-14, of the Lahaug reference, as a teaching of a plasma nitridation process; however, "reoxidation" and

nitridation are quite different processes. The Examiner might also be misinterpreting the discussion at column 4, lines 10-15, with regard to the reoxidized first gate oxide 28 incorporating the oxynitride 20, as a teaching of a second plasma nitridation process; however, any nitrogen incorporated into the reoxidized first gate oxide 28 is only a function of it being formed over the oxynitride 20. Accordingly, it is the Appellants' belief that the Examiner is misinterpreting the Lahaug reference.

Therefore, Lahaug does not disclose each and every element of the claimed invention and as such, fails to anticipate independent Claims 1 and 6. Because Claims 2-3 and 7 are dependent upon Claims 1 and 6, Lahaug also fails to anticipate Claims 2-3 and 7.

Rejection under 35 U.S.C. 103(a) over Lahaug in view of Chau

B. Rejection of Claims 4-5 and 8.

The Examiner has rejected Claims 4-5 and 8 under 35 U.S.C. §103(a) as being unpatentable over Lahaug as applied to Claims 1-3 and 6-7, and further in view of U.S. Patent No. 6,087,236 to Chau, *et al.* ("Chau"). The Appellants respectfully disagree since Lahaug fails to teach or suggest the element of performing a second plasma nitridation process on the second oxide layer and the first plasma nitrided oxide layer, with respect to Claim 1, and forming a second plasma nitrided oxide layer on the semiconductor substrate in the regions from which the first plasma nitrided oxide layer was removed, with respect to Claim 6, and Chau fails to correct the deficiencies of Lahaug.

The Appellants established in the section directly above that Lahaug fails to disclose the aforementioned claimed elements. Lahaug further fails to suggest these elements. Specifically, Lahaug fails to suggest these elements because Lahaug fails to teach that any other nitridation process occurs other than the first plasma nitridation process used to form the oxynitride 20 from the first gate oxide layer 18. As no other nitridation process occurs, the second gate oxide layer 30 can not be subjected to a nitridation process, as claimed in independent Claim 1, as well as the second gate oxide layer 30 can not be a second plasma nitrided oxide layer, as claimed in independent Claim 6. Accordingly, Lahaug fails to teach or suggest the aforementioned elements.

The Examiner is offering Chau for the sole proposition of incorporating less than 3 to 30 atomic percent of nitrogen into a dielectric layer. Without even addressing whether the Examiner's proposition is accurate, a teaching or suggestion of incorporating less than 3 to 30 atomic percent of nitrogen into a dielectric layer is significantly different from a teaching or suggestion of performing a second plasma nitridation process on the second oxide layer and the first plasma nitrided oxide layer, as recited in independent Claim 1, or of forming a second plasma nitrided oxide layer on the semiconductor substrate in the regions from which the first plasma nitrided oxide layer was removed, as recited in independent Claim 6. Accordingly, Chau also fails to teach or suggest these claimed elements.

Lahaug, individually or in combination with Chau, thus fails to teach or suggest the invention recited in independent Claims 1 and 6. Because Claims 4-5 and 8 are dependent upon Claims 1 and 6, the combination also does not render obvious Claims 4-5 and 8. The references, thus, fail to establish a prima facie case of obviousness with respect to these claims. Claims 4-5 and 8 are therefore not obvious in view of Lahaug and Chau.

For the reasons set forth above, the Claims on appeal are not anticipated by Lahaug. Further, the Claims are patentably nonobvious over the combination of Lahaug in view of Chau. Accordingly, the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellants' pending claims.

Respectfully submitted,

Hitt Gaines, P.C.


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Dated: 12-21-05

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VIII. APPENDIX A - CLAIMS

1. A method for forming MOS transistor gate dielectrics, comprising:
providing a semiconductor substrate;
forming a first dielectric layer on said semiconductor substrate;
performing a first plasma nitridation of said first dielectric layer;
removing said first dielectric from a region of said substrate;
forming a second dielectric layer on said semiconductor substrate in said region from
which said first dielectric layer was removed; and
simultaneously performing a second plasma nitridation of said second dielectric layer and
said first dielectric layer.
2. The method of claim 1 wherein said first dielectric layer comprises silicon oxide.
3. The method of claim 2 wherein said second dielectric layer comprises silicon oxide.
4. The method of claim 1 wherein said second dielectric layer has a final nitrogen
concentration of 5 to 15 atomic percent following said first and second plasma nitridation.
5. The method of claim 4 wherein said first dielectric layer has a nitrogen concentration
of 5 to 20 atomic percent following said second plasma nitridation.

6. A method for forming integrated circuit MOS transistors, comprising:
- providing a semiconductor substrate;
 - forming a first silicon oxide layer;
 - performing a plasma nitridation process on said first silicon oxide layer forming a first plasma nitrided oxide layer;
 - removing said first plasma nitrided oxide layer from regions of said substrate; and
 - forming a second plasma nitrided oxide layer on said semiconductor substrate in said regions from which said first plasma nitrided oxide layer was removed.
7. The method of claim 6 wherein said forming said second plasma nitrided oxide layer comprises:
- forming a second silicon oxide layer in said regions from which said first plasma nitrided oxide layer was removed; and
 - performing a second plasma nitridation process on said second oxide layer and said first plasma nitrided oxide layer.
8. The method of claim 7 wherein said first plasma nitrided oxide layer comprises 5 to 15 atomic percent of nitrogen.

IX. APPENDIX B - EVIDENCE

The evidence in this appendix includes Lahaug, Moore, Chau and JP No. 04154162. Lahaug was entered in the record by the Examiner with the First Examiner's Office Action on September 9, 2004. Moore, Chau and JP No. 04154162 were entered into the record by the Appellants by filing an IDS that was received by the USPTO on November 6, 2003.

X. RELATED PROCEEDINGS APPENDIX

NONE